Refine Search

Your wildcard search against 10000 terms has yielded the results below.

Your result set for the last L# is incomplete.

The probable cause is use of unlimited truncation. Revise your search strategy to use limited truncation.

Search Results -

Terms	Documents
L22 same map$ same redundant	5

Database:

US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L23

Refine Search

Recall Text Clear Interrupt

Search History

DATE: Monday, August 16, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
	DB=USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR		
L23	L22 same map$ same redundant	5	L23
L22	first same second same location same defective	1059	L22
L21	L13 same defective	6	L21
L20	l13 same first	15	L20
L19	L15 same l16	1	L19
L18	L16 same l15	1	L18
L17	L16 same l15 same map$	0	L17
L16	first adj1 defective	398	L16
L15	first adj1 location	22417	L15
L14	L13 same (row or column)	7	L14

L13	redundant same map$ same location same value	44	L13
DB=USPT; PLUR=YES; OP=OR			
L12	L11 same redundant	0	L12
L11	L10 same l9	11	L11
L10	second adj1 location	16243	L10
L9	L8 same l4	57	L9
L8	first adj1 location	18012	L8
L7	l4 same location	6536	L7
L6	L5 same l3	3	L6
L5	L4 same defective	251	L5
L4	value same map$	38803	L4
L3	redundant same row same column	2160	L3
L2	(4837520| 5406565| 5644529| 5677917| 5680354| 5796653| 5808944| 6317846| 6397349)![pn]	9	L2
L1	6671834[pn]	1	L1

END OF SEARCH HISTORY

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L18: Entry 1 of 1 File: USPT Sep 8, 1992

DOCUMENT-IDENTIFIER: US 5146571 A
**** See image for Certificate of Correction ****
TITLE: Remapping defects in a storage system through the use of a tree structure

Detailed Description Text (19):
A method and apparatus for producing the sorted defect list from a merged defect list is illustrated in the sort flow diagram of FIG. 5. The memory tables and memory registers employed in sorting the merged defect list to produce the final defect list are illustrated in FIG. 6. As illustrated in block 138 the "TR" register is initialized to point to the first address of the list to sort. Thereafter, the register "count" is loaded with the value from the first location in the final defect list which is pointed by the "TR" register. The "TR" register is then incremented to point to the fist defective physical address in the merged defect list. A second address Pointer "TMP", is initialized to point to the start of a temporary memory table. The value minus one (-1) is stored in the first location of the temporary memory table and the address pointer "TMP" is then incremented to point to the next location, address 1, in the temporary memory table. The first defective physical address in the merged defect list is then stored in address 1 of the temporary list. The address pointer "TR" is then incremented to point to the second defective physical address in the merged defect list. A loop counter is next set to a value of 1 thus completing the initialization procedure of block 138. Thereafter, commencing with block 140 an insertion sort is performed in which successive defective physical addresses from the merged defect list are successively inserted in the proper location in the temporary list. The insertion sort of FIG. 5 is specifically illustrated in FIG. 7 where the values of the respective variables of the sort flow diagram of FIG. 5 are illustrated in transforming the exemplary merged defect list of FIG. 4c into the sorted defect list of FIG. 4d.

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L23: Entry 4 of 5 File: USPT Nov 24, 1998

DOCUMENT-IDENTIFIER: US 5841709 A
TITLE: Memory having and method for testing redundant memory cells

Abstract Text (1):
A memory device includes an array of matrix memory cells that each correspond to a matrix location within the matrix array, an array of redundant memory cells that each correspond to a redundant location within the redundant array, and address and test circuitry. During a first test mode that is performed before any redundant cells have been mapped to the addresses of matrix locations, the address and test circuitry simultaneously addresses all of the matrix locations and selects all of the redundant memory cells. During a second test mode that is performed after the first test mode, the address and test circuitry simultaneously addresses all of the matrix locations and selects only those redundant memory cells that are mapped to the addresses of matrix locations. Typically, the redundant memory cells are so mapped to replace defective matrix memory cells.

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L6: Entry 3 of 3 File: USPT Feb 27, 1996

DOCUMENT-IDENTIFIER: US 5495447 A
TITLE: Method and apparatus using mapped redundancy to perform multiple large block memory array repair

Detailed Description Text (8):
Once defective cells are identified during testing, the redundancy circuit 20 is configured so that addresses of the defective cells map to portions of redundant memory. The redundancy circuit 20 includes storage devices 24 and 34, each for storing data from defective memory locations corresponding to one defect in a sub-array. Therefore, for a given memory array 11, the redundant circuitry described here is capable of providing redundant storage for two independent clusters of defective cells. The two clusters of defective cells may be in the same sub-array, or in two different sub-arrays. The configuration of redundant storage 24 and 34 is accomplished by fusing the appropriate bit values of the fusible address field 22 or 23. The mapping may be performed to provide either column redundancy or row redundancy or both concurrently as needed.

Detailed Description Text (21):
Referring again to FIG. 3, the redundancy circuit 20 further includes a fusible address fields 22 and 23 each for storing 8 bits of information. For example, fusible fields 22a and 23a identify whether the cluster of defective bits is mapped using column redundancy or row redundancy, where bit position 0 is here a `0` value indicates row redundancy, and a `1` value indicates column redundancy. Fusible fields 22b and 23b further include a 4 bit field which identifies the sub-array (14a-14p) in which there is a cluster of defective bits. Fusible fields 22c and 23c also include a 3 bit field which identifies which of the eight column or row groups (as shown in FIG. 2B) are stored in the redundant storage units 24 and 34.

Detailed Description Text (24):
The compare unit 26 generates a hit on any address which matches the fused addresses stored in fusible address fields 22 and 23. Due to the method of mapping bits into the redundant store, as described with reference to Table I and Table II, the bits of the fusible address fields 22 and 23 correspond to a specific subset of the address bits, and thus the compare of the two fields may be performed using a simple comparator. When using column redundancy, that is when the Row/Col fuse 22a is set to a `1` value, the fusible address bits 22b and 22c, which identify the defective array (0011) and the defective column group (101) respectively, correspond to the following bits of the address field: ##STR3##

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L6: Entry 2 of 3 File: USPT Aug 18, 1998

DOCUMENT-IDENTIFIER: US 5796653 A
** See image for Certificate of Correction **
TITLE: Circuit for the selection of redundant memory elements and flash EEPROM memory comprising said circuit

Detailed Description Text (25):
In cases of a scrambled mapping, where physical addresses differ from logical addresses, the incrementation value D may be 2 or 4, or dependant from a more complex scrambling function. In these cases, the incrementation value will be stored in a non-volatile register, with the configuration of scrambling parameters. This is the case for highly secured chips. In simple cases, the incrementation value will generally be one. When this happens (D=1), the invention reduces to replacement of defective pairs of adjacent rows or columns by a pair of redundant rows or columns.

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L6: Entry 1 of 3 File: USPT Jun 5, 2001

DOCUMENT-IDENTIFIER: US 6243305 B1
TITLE: Memory redundancy device and method

Brief Summary Text (11):
According to the present invention, there is provided a redundant circuit and method for a memory device having a plurality of row and column lines, including a programmable circuit for indicating at least one row or column line having a defect and a shifter circuit for shifting the memory addresses to bypass the at least one indicated defective row or column line. In particular, the shifter circuit modifies the address mapping for the row or column lines initially mapped to address values which are greater than the address value corresponding to the defective row or column line indicated by the programmable circuit. For each row or column line initially mapped to an address value which is greater than the address value corresponding to the defective row or column line, the shifter circuit maps a new address value to the row or column line which is one less than the address value initially mapped thereto. The highest numbered address values are mapped to a redundant row or column line. In this way, the defective row or column line is effectively bypassed.

Brief Summary Text (13):
In a first preferred embodiment of the present invention, the programmable circuitry is capable of indicating more than one defective row or column line in the memory device. Following the indication of at least two defective row or column lines in the memory device, for each row or column line initially mapped to an address value which is greater than a first address value corresponding to a first defective row or column line but less than a second address value corresponding to a second defective row or column line, the shifter circuit maps an address value to the row or column line which is one less than the address value initially mapped thereto. In addition, for each row or column line initially mapped to an address value which is greater than the second address value, the shifter circuit maps an address value to the row or column line which is two less than the address value initially mapped thereto. In this way, the address values which are greater than the first address value but less than the second address value are mapped to at least a next higher row or column line, and the address values which are greater than the second address value are twice shifted to higher row or column lines. The highest two address values are each mapped to a redundant row or column line. Consequently, both the first and second defective row or column lines are effectively bypassed.

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